**THIẾT KẾ HỆ THỐNG SỐ VỚI HDL**

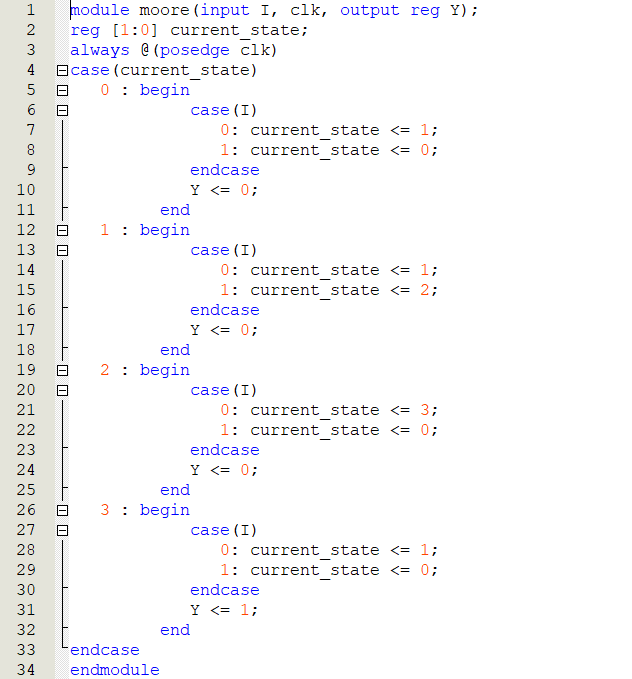
**BÀI THỰC HÀNH 3**

**GVHD:** Tạ Trí Đức

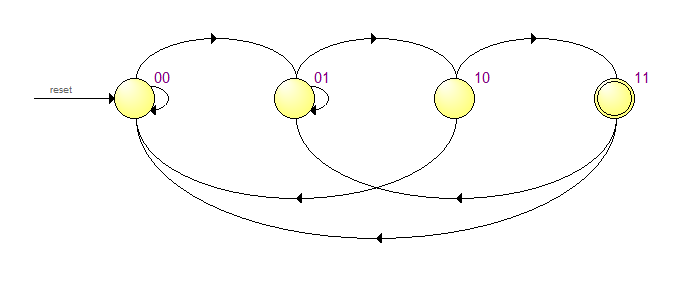
**Sinh viên thực hiện:** Phạm Quốc Tiến – 22521472

1. **Thiết kế mạch tuần tự**
   1. **Kiểu Moore**

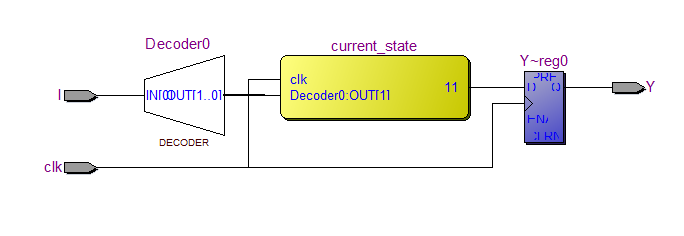
Code:



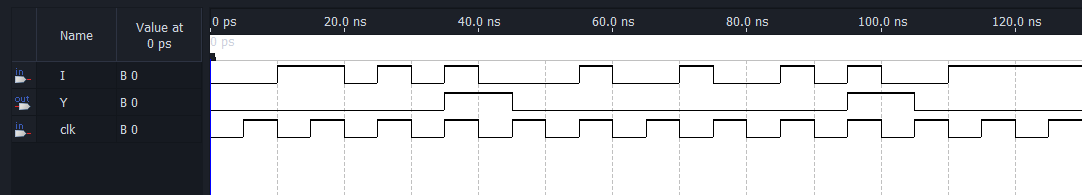
Sate machine:



RTL:

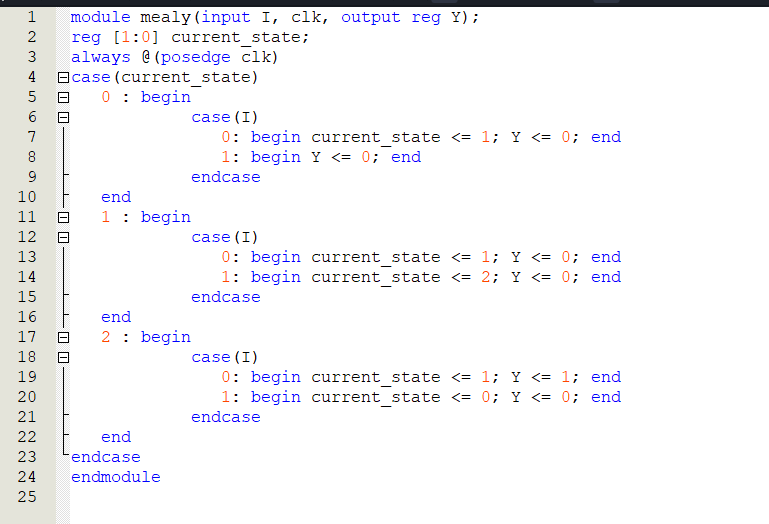


Waveform test function:

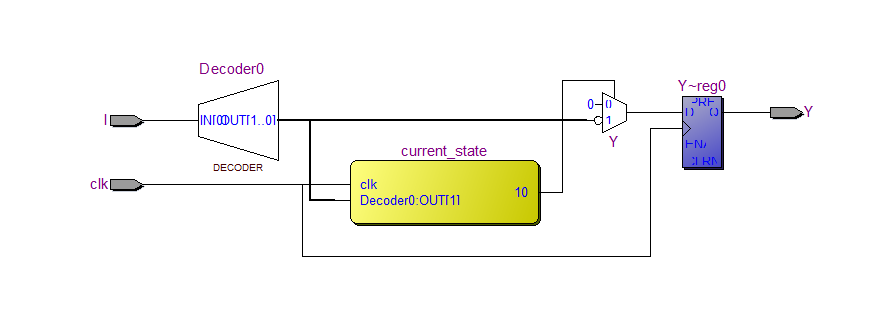


* 1. **Kiểu Mealy**

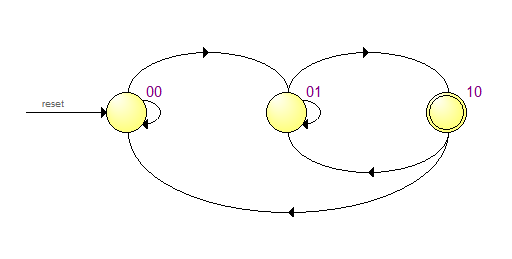
Code:



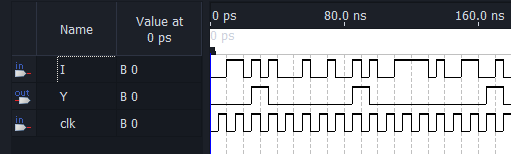
RTL:



State machine:

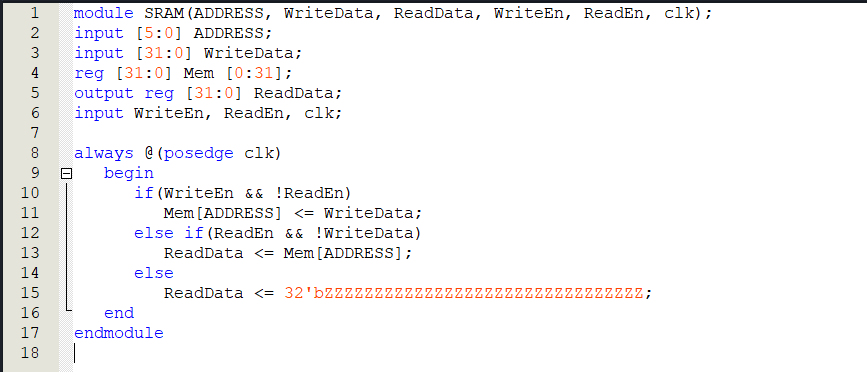


Waveform test function:

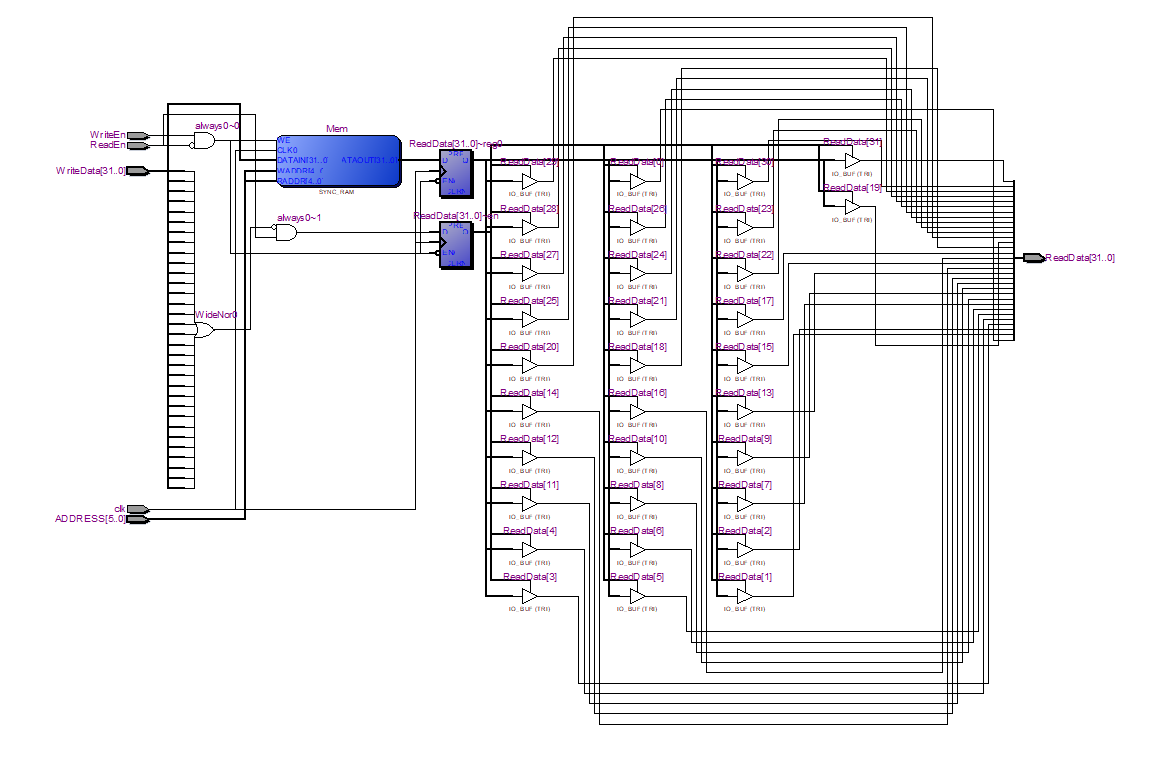


1. **Thiết kế bộ nhớ SRAM**

Code:



RTL:



Waveform test function:

